CLAIMS:

1. A method of operating a data processing device (100), notably a chip card, which includes an integrated circuit (10) which executes useful arithmetic operations, notably cryptographic operations, in dependence on a first clock signal, characterized in that a second clock signal is derived from the first clock signal under random control so as to be applied to the integrated circuit (10) instead of the first clock signal while distances between clock edges of the second clock signal vary at random in time.

2. A method as claimed in Claim 1, characterized in that the integrated circuit (10) is switched to different modes of operation under random control.

3. A method as claimed in Claim 2, characterized in that the various modes of operation include at least two calculation methods which produce an identical result while using different arithmetical approaches.

4. A method as claimed in ~~one of the Claims 2 or 3~~ Claim 3, characterized in that the various modes of operation include at least one mode of operation "dummy" (32) in which the integrated circuit (10) does not execute useful operations but dummy arithmetic operations which act on predetermined or random input data, the result being rejected and not taken up in the results or input data for the useful arithmetic operations.

5. A method as claimed in ~~one of the Claims 2 to 4~~ Claim 4, characterized in that the various modes of operation include a mode "deactivated" (36) in which the integrated circuit (10) does not execute arithmetic operations.

6. A data processing device (100), notably a chip card, which is specifically intended to carry out a method as claimed in at least one of the preceding Claims and includes an integrated circuit (10) which executes useful arithmetic operations, notably cryptographic operations, in dependence on the first clock signal (18), characterized in that the device is provided with a clock control unit (14) which is connected to the integrated

circuit (10) as well as with a random generator (12) which is connected to the clock control unit (14), the clock control unit (14) being constructed in such a manner that it generates a second clock signal (20) in dependence on the random generator (12) and the first clock signal (18), which second clock signal varies at random and controls the integrated circuit (10).

7. A data processing device (100) as claimed in Claim 6, characterized in that the clock control unit (14) is constructed in such a manner that it switches, (via control leads 28) and in dependence on the random generator (12), the integrated circuit (10) to various modes of operation (30, 32, 34, 36) on a random basis.

8. A data processing device (100) as claimed in Claim 7, characterized in that the various modes of operation (30, 32, 34, 36) include at least two calculation methods (30, 34) which produce an identical result while using different arithmetical approaches.

9. A data processing device (100) as claimed in ~~one of the Claims 7 or 8~~ Claim 8, characterized in that, the various modes of operation (30, 32, 34, 36) include at least one mode of operation "dummy" (32) in which the integrated circuit (10) does not execute useful operations but dummy arithmetic operations which act on predetermined or random input data, the result not being taken up in results or input data for the useful arithmetic operations.

10. A data processing device (100) as claimed in ~~one of the Claims 7 to 9~~ Claim 9, characterized in that the various modes of operation (30, 32, 34, 36) include a mode "deactivated" (36) in which the integrated circuit (10) does not execute arithmetic operations.

11. A data processing device (100) as claimed in ~~one of the Claims 7 to 10~~ Claim 10, characterized in that in at least one further mode of operation the time base (16) is additionally distorted so that the summing according to the "Differential Power Analysis" method is additionally impeded or made impossible.

LIST OF REFERENCES

100	data processing device
10	integrated circuit
12	random generator
14	clock control unit
16	horizontal axis t
18	signal $TAKT_1$
19	lead
20	signal $TAKT_2$
21	lead
22	signal DUMMY
24	signal DEAKT
26	signal ALT
28	control leads
29	line with modes of operation
30	mode of operation "method 1"
32	mode of operation "dummy"
34	mode of operation "method 2"
36	mode of operation "deactivated"
38	lead